Faculty of Engineering & Technology
KAKATIYA UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) VI SEMESTER

S. No.	Course Code	Course Title	Scheme of Instruction			Lecture hrs/week	Scheme of Examination		Credits
			L	T	P		CIE	SEE	
1	PC3201EC	Digital Signal Processing	4	0	0	4	30	70	4
2	PC3202EC	VLSI Design	4	0	0	4	30	70	4
3	PC3203EC	Data Communication and Computer Networks	3	0	0	3	30	70	3
4	PE-II*	Professional Elective–II	3	0	0	3	30	70	3
5	PE-III**	Professional Elective–III	3	0	0	3	30	70	3
6	OE-I#	Open Elective-I	3	0	0	3	30	70	3
8	PC3214EC	Digital Signal Processing Laboratory	0	0	3	3	25	50	1.5
9	PC3215EC	Electronic Design and Automation Laboratory	0	0	3	3	25	50	1.5
10	PW3216EC	Summer Internship***	6-weeks				-	-	-
	Total		**20**	**0**	**6**	**26**	**230**	**520**	**23**

***(PE-II) Professional Elective–II**
PE3204EC: Embedded System Design
PE3205EC: Artificial Neural Networks and Fuzzy Logic
PE3206EC: Adaptive Filter Theory and Applications
PE3207EC: Optical Communication

****(PE-III) Professional Elective–III**
PE3208EC: Information theory and Coding
PE3209EC: Wireless Communications
PE3210EC: Radar Engineering
PE3211EC: MOOCs Course

 # Please Refer Annexure

Faculty of Engineering & Technology
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B. Tech. (ECE) VI SEMESTER

PC3201EC DIGITAL SIGNAL PROCESSING

Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I
Introduction: Review of Discrete Time Fourier Transform, Concept of frequency in continuous and discrete time signals, DFT and its properties, linear convolution, circular convolution. Computational complexity of direct Computation of DFT, Fast Fourier Transform, DIT and DIF, FFT algorithms for RADIX-2 case, in-place computation, Bit reversal, Finite word length effects in FFT algorithms, Use of FFT in Linear Filtering.

UNIT-II
FIR Filters: FIR digital filter design techniques. Properties of FIR digital filters, design of FIR filters using windows and frequency sampling techniques, linear phase characteristics. Realization diagrams for IIR and FIR filters, finite word length effects.

UNIT-III
IIR Filters: Analog filter design – Butterworth and Chebyshev approximations, IIR digital filter design techniques, impulse invariant technique. Bilinear transform technique. Comparison of FIR and IIR filters, frequency transformations.

UNIT- IV
Multirate signal processing: Introduction, decimation by a factor D, interpolation by a factor I, sampling rate conversion by a rational factor I/D, design of practical sampling rate converter, S/W implementation of sampling rate converter, application of Multirate signal processing.

UNIT-V
DSP Processors: Introduction to Fixed point Digital Signal Processors, TMS 320C54XX processor-architecture, addressing modes, instruction set, Assembly programming, programming issues, Applications of DSP processors.

Suggested Readings:

1. John G.Proakis and Dimitris G. Manolakis, *"Digital Signal Processing principles, Algorithms and Applications"*, 3rd Edition, Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Alan V. Oppenheim and Ronald W. Schafer," Discrete *Time Signal Processing*", 3rd edition, Prentice Hall, Upper Saddle River, NJ,2010
3. Sanjit K. Mitra, "*Digital Signal Processing: A Computer-Based Approach*", 4/e, McGraw-Hill, New York,2011
4. Avatar sing and S.Srinivasan, *"Digital Signal Processing implementation using DSP Microprocessors with Examples from TMS320C54XX"*, Thomson Books Icole, 2004.

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B. Tech. (ECE) VI SEMESTER

PC3202ECVLSI DESIGN
Credits: 4

Instruction: 4 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT – I
Design Abstraction in Digital circuits, Fabrication process flow of nMOS and pMOS transistors, Overview of CMOS and BiCMOS technologies, MOSFET Transistor under static conditions, channel Length Modulation, Velocity Saturation, Sub-threshold Condition, Threshold variations, MOS structure Capacitance, CMOS Latch up, Technology scaling.

UNIT – II
CMOS Inverter, Voltage Transfer Characteristics, Static Power Consumption, Dynamic Power Consumption, Propagation Delay, Power-Energy and Energy-Delay Product, Layout Design of basic gates, Silicon on Insulation Technology, FinFET, Comparison of SOI and FinFET.

UNIT – III
Designing Combinational Logic gates in CMOS: Complementary CMOS, Ratioed Logic, Pass Transistor Logic, Dynamic CMOS logic-basic principle, Signal integrity issues in Dynamic Design, domino logic, np-CMOS logic, Merits and Demerits of above logic styles. Designing sequential logic: Bistability Principle, Multiplexer based latch, Dynamic latch, Pipelining.

UNIT – IV
Designing Arithmetic Building Blocks: Adder, Binary Adder, Full Adder, and Mirror Adder, Transmission gate-based Adder, Manchester Carry Chain Adder, Carry Bypass Adder, Carry Look ahead Adder, Carry Save Adder, Multiplier, Carry Save Multiplier, Barrel Shifter, and Logarithmic Shifter. Design of Memory Structures: ROM cells, PROM, EPROM, EEPROM, Flash Memory, SDRAM and DRAM.

UNIT – V
Implementation of strategies for Digital ICs, Testing of VLSI circuits: VLSI Chip Yield, Test procedures; Design for Testability- Ad Hoc Testing, Scan Based testing, Boundary Scan Design, Built in Self-Test, Built-in logic block observer, Test Pattern Generator, Automatic Test Pattern Generation (ATPG).

Suggested Readings:

1. JAN.M. Rabaey, A. Chandrakasan and B. Nikholic, *"Digital Integrated Circuits – A Design Perspective"*, 2nd Edition, PHI, 2007.
2. David A Hodges, H. Jackson and R. A. Saleh, *"Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology"*, 3rd Edition, Tata McGraw Hill, 2007.
3. John. P. Uymera, *"Introduction to VLSI Circuits and system"*, student edition, John Wiley and Sons, 2003.

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B. Tech. (ECE) VI SEMESTER

PC3203ECDATA COMMUNICATION AND COMPUTER NETWORKS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT - I

Data communication: A Communication Model, The Need for Protocol Architecture and Standardization, Network Types: LAN, WAN, MAN. Network Topologies: Bus, Star, Ring, Hybrid. Line configurations. Reference Models: OSI,TCP/IP.
Circuit switching: Circuit Switching Principles andconcepts.
Packet switching: Virtual circuit and Datagram subnets, X.25.

UNIT - II

Data Link Layer: Need for Data Link Control, Design issues, Framing, Error Detection and Correction, Flow control Protocols: Stop and Wait, Sliding Window, ARQ Protocols, HDLC. **MAC Sub Layer:** Multiple Access Protocols: ALOHA, CSMA, Wireless LAN. IEEE 802.2, 802.3, 802.4, 802.11, 802.15, 802.16 standards. Bridges and Routers.

UNIT - III

Network Layer: Network layer Services, Routing algorithms: Shortest Path Routing, Flooding, Hierarchical routing, Broadcast, Multicast, Distance Vector Routing, and Congestion Control Algorithms.
Internet Working: The Network Layer in Internet: IPV4, IPV6, Comparison of IPV4 and IPV6, IP Addressing, ATMNetworks.

UNIT - IV

Transport Layer: Transport Services, Elements of Transport Layer, Connection management, TCP and UDP protocols, ATM AAL Layer Protocol.

UNIT - V

Application Layer: Domain Name System, SNMP, Electronic Mail, World Wide Web. **Network Security:** Cryptography Symmetric Key and Public Key algorithms, Digital Signatures, Authentication Protocols.

Suggested Reading:

1. Andrew S Tanenbaum, *"Computer Networks,"* 5/e, Pearson Education,2011.
2. Behrouz A. Forouzan, *"Data Communication and Networking,"*3/e, TMH,2008.
3. William Stallings, *"Data and Computer Communications,"* 8/e, PHI,2004.
4. Douglas EComer, *"Computer Networks and Internet"*, Pearson Education Asia,2000.
5. PrakashC. Gupta, *"Data Communications and Computer Networks"*, PHI learning,2013

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE–II

PE3204EC EMBEDDED SYSTEM DESIGN

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT-I

Introduction to Embedded Systems: The Embedded Design Life Cycle - Product Specification, Hardware/Software Partitioning, Iteration and Implementation, Detailed Hardware (selection of processor) and Software Design, Hardware/Software Integration, Product Testing and Release, Maintenance and Upgradation.

UNIT-II

ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, ARM processor fundamentals, registers, current program status register, pipeline, exceptions, interrupts, and vector table, core extensions, architecture revisions, ARM processor families.

UNIT-III

Embedded processing with ARM CORTEX on Zynq: Fundamentals of FPGA, types of FPGA, case study of Xilinx FPGA, Processing System, programmable logic, programmable logic interfaces, security, Zynq 7000 family members, Zynq versus standard FPGA, Zynq versus standard processor.

UNIT-IV

Embedded Software Development Tools: Host and Target Machines, Cross Compilers, Cross Assemblers, Tool Chains, Linkers/Locators for Embedded Software, Address Resolution, Locator Maps. Getting Embedded Software into Target System: PROM programmer, ROM emulator, In Circuit- Emulators, Monitors, Testing on Your Host Machine - Instruction Set Simulators, Logic Analyzers.

UNIT-V

Introduction to Real Time Operating Systems: Tasks and task states, tasks and Data, Semaphores and shared data. Operating system services: Message queues, mailboxes and pipes, timer functions, events, memory management, Interrupt routines in an RTOS environment.

Suggested Readings:

1. Arnold S Berger, "*Embedded Systems Design*", South Asian edition, CMP Books, 2005.
2. Andrew Sloss, Dominic Symes, Chris Wright, *"ARM System Developer's Guide: Designing and Optimizing System Software"*, Elsevier, 2004.
3. Louise H Crockett, Ross.A.Elliot et *al " The Zynq Book*" , Edition 1, Strathclyde academic media, July 2014.
4. David E Simon, *"An Embedded software primer"*, Pearson, 2012

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

Unit –I

Introduction to Neural Networks: Introduction, Biological Neuron, Biological and Artificial Neuron Models, Characteristics of ANN, McCulloch-Pitts Model, Essentials of Artificial Neural Networks: Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Applications of ANN.

Unit- II

Feed Forward Neural Networks: Single Layer: Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.
Multilayer: Generalized Delta Rule, Derivation of Back propagation (BP) Training, Summary of Back propagation Algorithm, Kolmogorov Theorem

Unit–III

Associative Memories: Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory, Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem Architecture of Hopfield Network: Discrete and Continuous versions

Unit- IV

Classical & Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

Unit - V

Logic System Components: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods. Fuzzy logic applications

Suggested Readings:

1. James A Freeman and Davis Skapura, *"Neural Networks"*, Pearson Education, 2002.
2. B. Yeganaranarana, "*Artificial Neural Networks*", Prentice Hall, New Delhi, 2007.
3. Bart Kosko, "*Neural Networks and Fuzzy Logic System*", PHI Publications.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ADAPTIVE FILTER THEORY AND APPLICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT - I

Approaches to the development of adaptive filter theory. Introduction to filtering, smoothing and prediction. Wiener filter theory, introduction; Error performance surface; Normal equation; Principle of orthogonality; Minimum mean squared error; example.

UNIT - II

Gradient algorithms; Learning curves; LMS gradient algorithm; LMS stochastic gradient algorithms; convergence of LMS algorithms.

UNIT - III

Applications of adaptive filter to adaptive noise cancelling, Echo cancellation in telephone circuits and adaptive beam forming.

UNIT - IV

Kalman Filter theory; Introduction; recursive minimum mean square estimation for scalar random variables; statement of the kalman filtering problem: the innovations process; Estimation of state using the innovations process; Filtering examples.

UNIT V

Vector Kalman filter formulation. Examples. Application of kalman filter to target tracking.

Suggested Reading:

1. Sophoclas, J. Orphanidies, *"Optimum signal processing an introduction"*, McMillan, 1985.
2. Simon Haykins, *"Adaptive signal processing"*, PHI, 1986.
3. Bernard Widrow, *"Adaptive signal processing"*, PHI, 1986.
4. Bozic. SM., *"Digital and Kalman Filtering"*.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3207EC OPTICAL COMMUNICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT -I
Overview of Optical Fiber Communication: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, basic optical laws, Ray theory, step index and graded index fibers, ray optics representation, fiber materials.

UNIT - II
Transmission Characteristics of Optical Fibers: Introduction, Attenuation, absorption, scattering losses, bending loss, dispersion, Intra modal dispersion, Inter modal dispersion.

UNIT - III
Optical Sources and Detectors: Introduction, LED's, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors.

UNIT - IV
Fiber Couplers and Connectors: Introduction, fiber alignment and joint loss, fiber splices, fiber connectors and fiber couplers.
Optical Receiver: Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection.

UNIT –V
Analog and Digital Links: Analog links – Introduction, overview of analog links, CNR, Digital links – Introduction, point–to–point links, System considerations, link power budget, resistive budget.
WDM Concepts and Components: WDM concepts, overview of WDM operation principles, WDM standards,

Suggested Reading:
1. Optical Fiber Communication – Gerd Keiser, 4th Ed., MGH, 2008.
2. Optical Fiber Communications– – John M. Senior, Pearson Education, 2007.
3. Fiber optic communication – Joseph C Palais: 4th Edition, Pearson Education.

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B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –III

PE3208EC INFORMATION THEORY AND CODING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT - I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies. Channel Coding Channel capacity, binary symmetric channel, binary erasure channel, Shannon's channel coding theorem, Huffman coding.

UNIT - II

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - III

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT - IV

Convolutional Codes: Encoding of Convolutional Codes- Structural and Distance Properties, state, tree, trellis diagrams, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT - V

BCH Codes: Minimum distance and BCH bounds, Decoding procedure for BCH codes, Syndrome computation and iterative algorithms, Error locations polynomials for single and double error correction.

Suggested Readings:

1. K. Sam Shanmugam, "*Digital and analog communication systems*", John Wiley India Pvt. Ltd, 1996.
2. Simon Haykin, "*Digital communication*", John Wiley India Pvt. Ltd, 2008.
3. Muralidhar Kulkarni, K.S. Shivaprakasha, "*Information Theory and Coding*", Wiley India Pvt. Ltd, 2015, ISBN: 978-81-265-5305-1.
4. Shu Lin, Daniel J. Costello, Jr, "*Error Control Coding- Fundamentals and Applications*", Prentice Hall, Inc 2014.
5. Man Young Rhee, "*Error Correcting Coding Theory*" McGraw – Hill Publishing 1989

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PROFESSIONAL ELECTIVE –III

PE3209EC WIRELESS COMMUNICATIONS

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I

Overview of wireless communication system, History of wireless communication, current wireless systems, wireless spectrum, 2G, 3G, 4G and 5G wireless communication standards.

UNIT-II (Qualitative treatment only)

Comparison of digital Modulation schemes: Information Capacity, Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Band Width Efficiency.

UNIT-III

The wireless communication environment, classification of fading channels, different parameters related to fading mechanisms, modeling of wireless systems, system model for narrowband signals, Rayleigh fading wireless channel.

UNIT-IV

Basics mechanism of Code division multiple access (CDMA), fundamentals of CDMA codes, Introduction to MIMO wireless communication systems, MIMO system model, MIMO zero forcing and MMSE receiver.

UNIT-V

Multi carrier modulation, data transmission using multiple carriers, basics of orthogonal frequency division multiplexing (OFDM) systems, cyclic prefix, MIMO-OFDM system

Suggested Readings:

1. A. K. Jagannatham, *Principles of modern wireless communications systems*. McGraw Hill Education, 2015.
2. A. Goldsmith, *Wireless Communications*. New York: Cambridge Univ. Press, 2005.
3. T. S. Rappaprt, Wireless communications principles & Practices, Pearson, 2010.

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PROFESSIONAL ELECTIVE –III

PE3210EC RADAR ENGINEERING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 marks *SEE: 70 marks*

UNIT-I

Basics of Radar: Introduction, Maximum Unambiguous Range, Simple form of Radar Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications, Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation.

UNIT-II

CW and Frequency Modulated Radar: Doppler Effect, CW Radar – Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar, Illustrative Problems.FM-CW Radar, Range and Doppler Measurement, Block Diagram and Characteristics (Approaching/ Receding Targets), FM-CW altimeter, Multiple Frequency CW Radar.

UNIT-III

MTI and Pulse Doppler Radar: Introduction, Principle, MTI Radar with – Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancellers – Filter Characteristics, Blind Speeds, Double Cancellation, And Staggered PRFs. Range Gated Doppler Filters, MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler radar.

UNIT-IV

Tracking Radar: Tracking with Radar, Sequential Lobing, Conical Scan, Monopulse Tracking Radar –Amplitude Comparison Monopulse (one- and two- coordinates), Phase Comparison Monopulse, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers.

UNIT-V

Detection of Radar Signals in Noise: Introduction, Matched Filter Receiver – Response Characteristics and Derivation, Correlation Function and Cross-correlation Receiver, Radar Receivers: Noise Figure and Noise Temperature, Displays – types. Duplexers – Branch type and Balanced type, Introduction to Phased Array Antennas.

Suggested Readings:

1. Introduction to Radar Systems – Merrill I. Skolnik, TMH Special Indian Edition, 2nd Edition, 2007.
2. Introduction to Radar Systems – Merrill I. Skolnik, 3rd Edition, Tata McGraw-Hill, 2001.
3. Radar Principals, Technology, Applications – Byron Edde, Pearson Education, 2004.
4. Radar Principles – Peebles, Jr., P.Z.Wiley, NewYork, 1998.

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B. Tech. (ECE) VI SEMESTER

PC3214ECDIGITAL SIGNAL PROCESSING LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE:3 hours*
CIE: 25 Marks *SEE: 50 Marks*

List of Experiments

1. (a)Generation of basic signals based on recursive difference equations.
   (b) Operations on Basic sequences
2. (a) Linear and Circular Convolutions in time domain and frequency domain
   (b) Determination of autocorrelation and Power Spectrum of a given signal(s)
3. (a) Fast Fourier Transform – DIT and DIF algorithm
   (b) Spectrum analysis using DFT
4. (a) Generation of windows – Rectangular, Hamming and Hamming window
   (b) Design of LPF, HPF, BPF and BSF using windowing technique
5. (a) Design of Butterworth Filter using Impulse Invariant and Bilinear transformation
   (b) Design of Chebyshev Filter using Impulse Invariant and Bilinear transformation
6. (a) Implementation of Decimation and Interpolation Process.
   (b) Implementation of I/D sampling rate converters.
7. (a) Study of TMS320C54X DSP processor
   (b) Arithmetic operation using TMS320C54XX
8. MAC operation using various addressing modes
9. (a) Linear Convolution
   (b) Circular Convolution
10. (a) FFT Implementation
    (b) Waveform Generation – Sine wave and Square wave
11. Implementation of FIR filter on DSP processor
12. Implementation of IIR filter on DSP processor

Suggested Readings:

1. Digital Signal Processing Using. **MATLAB**, Third Edition. Vinay K. Ingle and John G. **Proakis**

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B. Tech. (ECE) VI SEMESTER

PC3215ECELECTRONIC DESIGN AND AUTOMATION LABORATORY

Credits: 1.5

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 25 Marks *SEE: 50 Marks*

List of Experiments:

Part A (Digital VLSI front-end Design)

1. Develop VERILOG HDL code and Test bench for the following:
   a. Multiplexer, Decoder, Encoder, Parity Generator, D flip-flop, four-bit adder and magnitude comparator using structural modelling
   b. Four-bit parallel adder/subtractor, zero/one detector and JK flip-flop using data flow modelling
   c. Arithmetic and logic unit, D, SR and JK flip-flops with synchronous and asynchronous resets, universal shift register and BCD- seven segment decoder using behavioral modelling
   d. Asynchronous, Synchronous, Ring and Johnson counters.
   e. Sequence Detector using Mealy and Moore type state machines.
2. Develop VERILOG HDL code for eight to three priority encoders using structural modelling and develop a test bench to cover all the functionalities. Assume each gate has a zero delay and three-simulation units delay.
3. Develop VERILOG HDL code for a four-bit carry look-ahead adder in structural modelling. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.
4. Develop VERILOG HDL code for four to sixteen decoder using two-to-four decoders and other combinational logic. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.
5. Using conditional operator, write Verilog HDL code to shift input *data* right arithmetic by the number of positions specified by another input *shift*. Develop test bench to cover all the functionalities.
6. Write Verilog HDL code to realize all bit Zero/One detector. Develop test bench to cover all the functionalities.
7. Develop Verilog HDL code to realize a MOD-10 synchronous decimal up counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
8. Develop VERILOG HDL code for the state machine of control unit of GCD processor.
9. Develop Verilog HDL code to realize a four-bit universal shift register. Develop test bench to cover all the functionalities.
10. Develop Verilog HDL code to realize a four-bit ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
11. Develop Verilog HDL code to realize a four-bit twisted ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.
12. Design a clock generator where its output *clk* is initialized to 0 and has a period of 500-time units and a duty cycle of 70 %.

13. Design four-bit binary to Gray converter and Gray to binary converter.

14. Acquaint with Synthesis and FPGA porting of the code.

Part B (Digital VLSI back-end Design)

1. Design and analyze the following CMOS circuits:
    a. Inverter using static, ratioed, dynamic and domino logic styles
    b. Two-input NAND gate
    c. Two-input NOR gate
    d. Two-to-one Multiplexer using transmission gate
    e. Design a one-bit full adder circuit
    f. Design a one-bit SRAM cell.
2. Draw the layout and evaluate the performance of CMOS Inverter and two-input CMOS NAND gate.

Suggested Readings:

1. Samir Palnitkar, "*Verilog HDL A Guide to Digital Design and Synthesis,*" 2nd Edition, Pearson Education, 2006.
2. Ming-Bo Lin, "Digital System Designs and Practices: Using Verilog HDL and FPGA," Wiley India Edition, 2008.
3. John P.Uyemura "Introduction to VLSI Circuits and Systems" John Wiley & Sons, ISBN No: 9971-51-417-6, 2002.
4. Neil H E Weste and David Money Harris, "CMOS VLSI design: A circuits and systems perspective" 4th Edition, Pearson, 2015.

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B. Tech. (ECE) VI SEMESTER

PW3216EC SUMMER INTERNSHIP

Credits: 0

Instruction: 6 weeks *Duration of SEE: --*
CIE: 50 *SEE: ---*

Summer Internship is introduced as part of the curricula for encouraging students to work on problems of interest to industries. A batch of two or three students will be attached to a person from an Electronics Industry / R & D Organization / National Laboratory for a period of 8 weeks. This will be during the summer vacation following the completion of the VI semester course. One faculty member will act as an internal guide for each batch to monitor the progress and interacts with the Industry guide.

After the completion of the project, students will submit a brief technical report on the project executed and present the work through a seminar talk to be organized by the department. Award of sessionalsare to be based on the performance of the student at the work place to be judged by industry guide and internal guide (25 Marks) followed by presentation before the committee constituted by the department (25 Marks). One faculty member will coordinate the overall activity of Summer Internship.

Annexure

- ✓ Students should not choose same department subject as an Open elective subject.
- ✓ Students can select any one of the following subjects as an Open elective subject.

Open Elective subjects offered from different department

Sl.No	Course Code	Name of the subject	Branch
1	OE3213EC	Microprocessor and Interfacing	ECE
2	OE3207CS	Fundamentals of Data Structures	CSE

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B. Tech. (ECE) VI SEMESTER

OPEN ELECTIVE-I

OE3213EC MICROPROCESSORS AND INTERFACING

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT I
Evolution of microprocessors, 8085 microprocessor architecture, addressing modes and instruction sets. Basic assembly language programming, pin configuration, timing diagram of read and write operation.

UNIT II
8086 architecture-functional block diagram, register organization, memory segmentation, programming model, pins description in maximum mode and minimum mode, timing diagrams.

UNIT III
Instruction formats, addressing modes, classification of instruction set, assembler directives, macros, 8086 microprocessor assembly language programs: simple programs involving data transfer operation, arithmetic operation, logical operation, branch operation, machine control operation, string manipulations, stack and subroutine operations.

UNIT IV
8255 Programmable peripheral interfaceblock diagram and various modes of operation. Interfacing of ADC, DAC, keyboard, seven segment display, stepper motor interfacing and 8254 (8253) programmable interval timers.

UNIT V
Interrupt structure of 8086, interfacing programmable interrupt controller 8259 and DMA Controller 8257 to 8086 microprocessor. Serial communication standards, RS 232,Serial data transfer schemes and block diagram of 8251 USART.

Suggested Readings:
1. Ramesh Gaonkar, "Microprocessor architecture, programming and applications with the 8085",Penram International Publication (India) Pvt. Ltd.
2. Douglas V. Hall, "Microprocessors and Interfacing", Tata McGraw Hill Publication.
3. Sivarama P. Dandamudi, "Introduction to Assembly Language Programing From 8086 to Pentium Processors", Springer Publication.
4. Walter A. Triebel and Avtar Singh, "The 8088 and 8086 Microprocessors: Programming, Interfacing Software, Hardware and Applications", Pearson Publication.
5. A. K. Ray and K. M. Bhurchandi, "Advance microprocessors and Peripherals" Tata McGraw Hill Publication.
6. Lyla B. Das, "The X86 Microprocessors, Architecture, Programming and Interfacing (8086 to Pentium)", Pearson Publication.

Faculty of Engineering & Technology
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B. Tech. (ECE) VI SEMESTER

OPEN ELECTIVE – I

OE3207CS FUNDAMENTALS OF DATA STRUCTURES

Credits: 3

Instruction: 3 periods per week *Duration of SEE: 3 hours*
CIE: 30 Marks *SEE: 70 Marks*

UNIT-I

Introduction: Introduction to data structure, types of data structures, revision of arrays, memory representation of arrays, operations on arrays, static versus dynamic memory allocation, pointers, self-referential Structure Time complexity.

UNIT-II

Stack-Queue (Linear Data structures): Definition of stack, operations on stack, implementation of stack. Applications of Stack.

UNIT-III

Definition of queue, operations on queue, implementation of queue using arrays
Applications of queue, Circular queue and priority queue.

UNIT-IV

Trees-Graphs (Nonlinear Data structures): definition of trees, Terminology on trees, binary tree, binary search tree and its operations, tree traversal techniques. Applications of Trees.

UNIT-V

Graph: definition, terminology on graphs, representation of graphs, graph traversal techniques, spanning tree, minimum cost spanning tree algorithms. Applications of Graphs.

Text Books:

1.Sahni Horowitz, “Fundamentals of data structures in C”, UniversitiesPress, second edition, 2008, ISBN No- 978-8173716058.
2.R Venkatesan,S Lovelyn Rose,“Data structures”,Wiley, second edition, 2019, ISBN No-978-8126577149.

References:

1.Narasimha Karumanchi, “Data Structures and Algorithms Made Easy: Data Structures and Algorithmic Puzzles”, Careermonk Publications, 2016, ISBN-No: 978-8193245279.

ABBREVIATIONS

L	:	Lectures	T	:	Tutorials
P	:	Practicals	CIE	:	Continuous Internal Evaluation
SEE	:	Semester End Examination	PC	:	Professional Core
OE	:	Open Elective	PW	:	Project Work

**Students have to undergo summer internship of 6 Weeks duration at the end of semester VI and valuation will be done in VII semester.